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(54) Digital bus control system.

(57) Digitally controllable ICs 1, 2, 3 in an electronic equipment are connected through control bus lines. Switch means is provided for disconnecting one of the digitally controllable IC from the control bus. The control bus is not disabled when such IC is turned off or is not occupied when the IC is operating in its internal processing mode. The communication between the remaining ICs through the control bus can be kept enabled.

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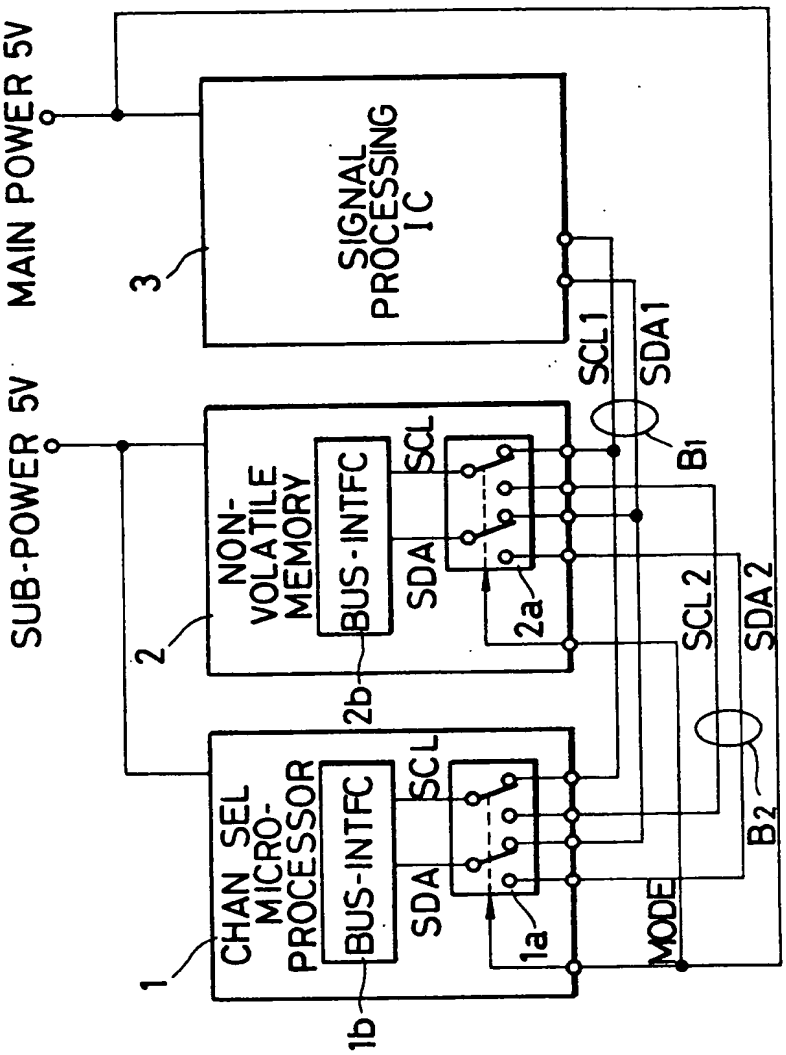
FIG. 1


MAIN POWER 5V
SUB-POWER 5V
SIGNAL PROCESSING I C
3
NON-VOLATILE MEMORY
BUS-INTFC
SCL
SDA
2
2a
2b
CHAN SEL MICRO-PROCESSOR
BUS-INTFC
SCL
SDA
1
1a
1b
SCL1
SDA1
B1
SCL 2
SDA 2
B2
MODE

DIGITAL BUS CONTROL SYSTEM

The present invention relates to a digital control bus system wherein function blocks included in electronic equipment are connected through bus lines to allow signal transmission therebetween. More particlarly, the present invention relates to a digital control bus system which inter-connects digitally controllable ICs installed in an electronic equipment.

Most video/audio equipment such as television receivers, VTRs, and tape recorders that use digitally controllable ICs employ an inner bus system. In a conventional inner bus system, electronic equipment includes a CPU, an inner bus, and a ROM as a control block. The control program for the respective circuits is stored in the ROM. In normal operation, the program is read out by the CPU and control signals are supplied to a predetermined circuit through the inner bus so that the corresponding digitally controllable IC performs a predetermined operation. These ICs are also controlled by a keyboard or a remote controller through the CPU and the inner bus.

A conventional inner bus is described as a two-line system consisting of a data transmission line and a clock transmission line in Japanese Patent Application laid open No. 57-106262.

For example, in a conventional TV set utilizing an inner bus system, a channel selection microprocessor, a non-volatile memory for storing control data, and a signal processing IC including a video processor and an audio processor are connected through a two-line inner bus. If a channel selection command is externally supplied to the TV set, the channel selection microprocessor reads out present data corresponding to the selected channel from the memory and transmits the present data to the signal processing IC. The channel selection microprocessor thus performs channel selection so as to receive a predetermined reception signal.

In another conventional VTR built-in TV set as a kind of composite video/audio equipment utilizing an nner bus system, a TV block and a VTR block are controlled by a key/remote controller decoder of a microprocessor through an inner bus.

In the above inner bus systems, an inner bus is commonly used in single electronic equipment. The bus is used (occupied) by time division processing. The bus cannot be used for simultaneous processing. For this reason, various operational limits and inconvenience result.

In the above TV set with the remote controller function, the channel selection microprocessor and the non-volatile memory are always supplied with an operating power from a subsidiary power supply. A main operating power is supplied to the signal processing IC upon ON/OFF operation of the power switch in a remote commander. In a remote controller standby mode, the main power to the signal processing IC is off to OV or grounded and the TV set waits to receive an operation command from the remote commander.

In this state, the common inner bus is also grounded and the channel selection microprocessor cannot access the non-volatile memory through the inner bus. For example, if the signal processing IC has a surge protection diode at an input end connected to the inner bus, the cathode of the protection diode connected to the power source is grounded, and the inner bus is thereby grounded.

Once the remote controller standby mode is set after, e.g., a power failure, a "last power flag" representing the TV operation mode immediately prior to the power failure cannot be read out from a memory area at the corresponding address of the non-volatile memory. As a result, the status prior to the power failure cannot be restored.

In the VTR built-in TV set, while the TV block occupies the bus to perform internal processing, the key/remote controller decoder cannot send a signal to the VTR block. In addition, the VTR block cannot use the inner bus to perform its internal processing.

Furthermore, the following problem also exists due to common use of the bus. A master controller sends both data and address signals for designating a slave device. In this case, if signal processing ICs (e.g., tuner ICs) having identical slave address in the TV and VTR blocks are provided, confusion should occur.

It is, therefore, an object of the present invention to improve utilization efficiency of the inner bus system while the inner bus disable state is prevented.

In order to achieve the above object of the present invention, there is provided a digital control bus system for exchanging signals between function blocks (1, 2, 3) through bus lines (SDA1, SCL1), comprising switch means (e.g., bus selection switches 1a and 2a) for effectively disconnecting a predetermined function block (e.g., a signal processing IC3) from the bus lines when the predetermined function block is powered off. With this arrangement, since the bus lines are not grounded, communication between the remaining function blocks can be guaranteed despite the predetermined function block having been powered off.

Fig. 1 is a block diagram of an inner bus system TV set according to an embodiment of the present invention;

Fig. 2 is a block diagram of a VTR built-in TV according to another embodiment of the present invention;

Fig. 3 is a block diagram of a bus switching system according to still another embodiment of the present invention; and

Fig. 4 is a block diagram of a bus disconnection system according to still another embodiment of the present invention.

Fig. 1 shows an inner bus system TV set according to an embodiment of the present invention. An inner bus employs a double bus system consisting of first and second buses B1 and B2. The bus B1 consists of a data/address line SDA1 and a clock line SCL1. Similarly, the bus B2 consists of a data/address line SDA2 and a clock line SCL2. The bus B1 is commonly connected to a channel selection microprocessor 1, a non-volatile memory 2, and a signal processing IC 3. The bus B2 is commonly connected to the channel selection microprocessor 1 and the non-volatile memory 2.

Bus selection switches 1a and 2a are arranged in the channel selection microprocessor 1 and the non-volatile memory 2, respectively. The channel selection microprocessor 1 and the non-volatile memory 2 are selectively connected to either one of the buses through bus interfaces (BUS-INTFCs) 1b and 2b.

A 5V sub-power supply is supplied to the channel selection microprocessor 1 and the non-volatile memory 2. The signal processing IC 3 is operated with a main power supply of 5 V.

When the TV set is operated upon TV signal reception, a mode signal MODE representing power-on state is set at logic "1". In response to this signal, the bus selection switches 1a and 2a select the first bus B1 (SDA1 and SCL1), as shown in Fig. 1. Therefore, TV signal reception is controlled through the first bus B1.

In the remote controller standby mode, the main power of 5 V is no longer supplied to the signal procesing IC 3 and the mode signal goes to logic "0". The channel selection microprocessor 1 and the non-volatile memory 2 are supplied by the sub-power supply and held in the wait mode. In this case, the first bus B1 is also grounded upon power-off of the signal processing IC3 and cannot be used.

However, the bus selection switches 1a and 2a are switched in response to the mode signal of logic "0" so that the channel selection microprocessor 1 can communicate with the non-volatile memory 2. Therefore, even in the standby mode, the channel selection microprocessor 1 can read out data from the non-volatile memory 2. For example, the "last power flag" can be read out upon recovery from the power failure to restore the operation status immediately prior to the power failure.

It will be apparent from the foregoing that, on entering the powered-down mode, the signal processing IC3 is disconnected from the currently active bus (i.e. bus B2) by the switches 1a and 2a switching over from bus B1 to bus B2.

Fig. 2 shows another embodiment of the present invention. This embodiment exemplifies a TV + VTR combination product. A TV block 5 comprises a channel selection microprocessor 1, a non-volatile memory 2, and a signal processing IC 3 in the same manner as in Fig. 1. A VTR block 6 comprises a channel selection microprocessor 11, a servo controller 12, and a signal processing IC 13.

Each of the TV and VTR blocks 5 and 6 has a double bus system consisting of buses B1 and B2 in the same manner as in Fig. 1. The intrablock communication paths can be enabled even in the remote controller standby mode.

In addition, a high-order double bus system is also employed in the entire system. The bus from the key/remote controller decoder 8 as a controller consists of a first bus IB1 for TV block and a second bus IB2 for VTR block. Each of the buses IB1 and IB2 is branched into parallel buses B1 and B2 in each blocks 5 and 6 in the same manner with Fig. 1.

The bus IB1 consists of a data/address line SDA3 and a clock line SCL3. Similarly, the bus IB2 consists of a data/address line SDA4 and a clock line SCL4. The first and second buses IB1 and IB2 are switched by a bus selection switch 8a in the key/remote controller decoder 8 and connected to the internal circuit in the decoder 8 through a bus interface (BUS INTEC) 8B. An operation signal - (control code) from a key matrix 14 on an electronic equipment panel surface or a remote controller receiver 15 is supplied to the decoder 8 through a decode circuit 8C and the bus interface 8b. At the same time, the decode circuit 8c outputs a TV/VTR mode signal upon operation of the key matrix 14 or the remote controller to cause the bus selection switch 8a to select one of the buses IB1 and IB2.

For example, the VTR is operated in the play mode in the following manner. The operator uses the key matrix or the remote controller to set the TV set in the VTR mode. In this case, the selection switch 8a is switched to the side of the first bus IB1. In this mode, the TV block 5 can receive a video RF signal. When the VTR is subsequently set in the play back mode, the selection switch 8a is switched to the side of the second bus IB2 and thus the VTR block 6 is set in the play back mode.

The TV and VTR blocks 5 and 6 can be controlled by the decoder 8 through the independent buses IB1 and IB2. Even if the TV block 5 continuously occupies the bus IB1 to perform its internal processing in the TV block 5, the communication path between the decoder 8 and the VTR block 6 is guaranteed through the bus IB2. Even if the ICs of an identical slave address are used in the TV and VTR blocks 5 and 6, the buses IB1 and IB2 are switched to easily identify the target slave device.

Fig. 3 shows still another embodiment of the present invention. The bus system in this embodiment is a compromise bus system between the double bus system of Fig. 1 and the exclusive bus system of Fig. 2. The inner bus (SDA and SCL) connected to a bus interface 1b in a channel selection microprocessor 1 is branched from a bus selection switch 1a into first and second buses B1 an dB2 which are connected to a signal processing IC3 and a non-volatile memory 2. The bus selection switch 1a is controlled in response to a switching signal SW1 to selectively form independent communication paths by using the buses B1 and B2 as exclusive buses for the function blocks (3 and 2). For example, the ON/OFF of the main power is detected according to the operation mode to form the switching signal SW1 which is used to disconnect the bus B1 of the signal processing IC3 from the channel selection microprocessor 1 and the non-volatile memory 2.

Bidirectional switches 1c and 1d are arranged to short-circuit both the data/address lines SDA1 and SDA2 and both the clock lines SCL1 and SCL2 of the first and second buses B1 and B2, respectively. If the bidirectional switches 1c and 1d are turned on in response to a switching signal SW2, the buses B1 and B2 function as an integral bus which can be used as a common inner bus in the electronic equipment.

In order to disconnect the common bus line from a predetermined function block, a disconnection switch 17 shown in Fig. 4 may be arranged accordingly to still another embodiment. For example, when the 5V main power is no longer supplied to the IC 3 in the remote controller standby mode, the disconnection switch 17 is opened and a function block 18a can be disconnected from the common bus lines SA and SCL connected to another function block 18b. The disconnection switch 17 may be a switching element included in the function block 18a and may serve as a high impedance when the main power is off.

The present invention is not limited to the particular embodiments described above but can also be applied to a certain inner bus system having a timer standby function, for example.

According to the present invention as described above, when a predetermined function block is powered off, it is disconnected from the bus line. Therefore, the bus line is not forcibly grounded in the power off state. The communication between the remaining function blocks can be guaranteed.

Claims

1. Digital control bus system applied to an electronic equipment, comprising

a control bus provided for connecting function blocks of said electronic equipment in order to transmit control data among said function blocks, and

switch means provided at said control bus for effectively disconnecting at least one of said function blocks from said control bus.

2. A digital control bus system according to claim 1, wherein said switch means is controlled in response to a main power supply applied to said one of function blocks.

3. A digital control bus system according to claim 1, wherein said electronic equipment has first control bus and second control bus and said switch means is operative to switch said one of function blocks from said first control bus to said second control bus.

4. A digital control bus system according to claim 3, wherein said orfe of function blocks includes said switch means between a bus interface and connecting terminals provided in said function block.

5. A digital control bus system according to claim 4, wherein said one of function blocks further includes switch means which connects said first control bus with said second control bus.

6. A digital control bus system according to claim 5, wherein said latter mentioned switch means is provided between said first mentioned switch means and said connecting terminal of the function block.

7. A digital control system according to claim 1 wherein two buses are provided, said at least one function block being connected to one of the buses and the switch means being operable to selectively connect the other of the function blocks to the other one of the buses, thereby to effectively disconnect said at least one function block.

8. A digital control system according to claim 1, wherein the switch means is interposed between the at least one function block and the bus and is arranged to open to disconnect said at least one function block from the bus.

FIG. 1

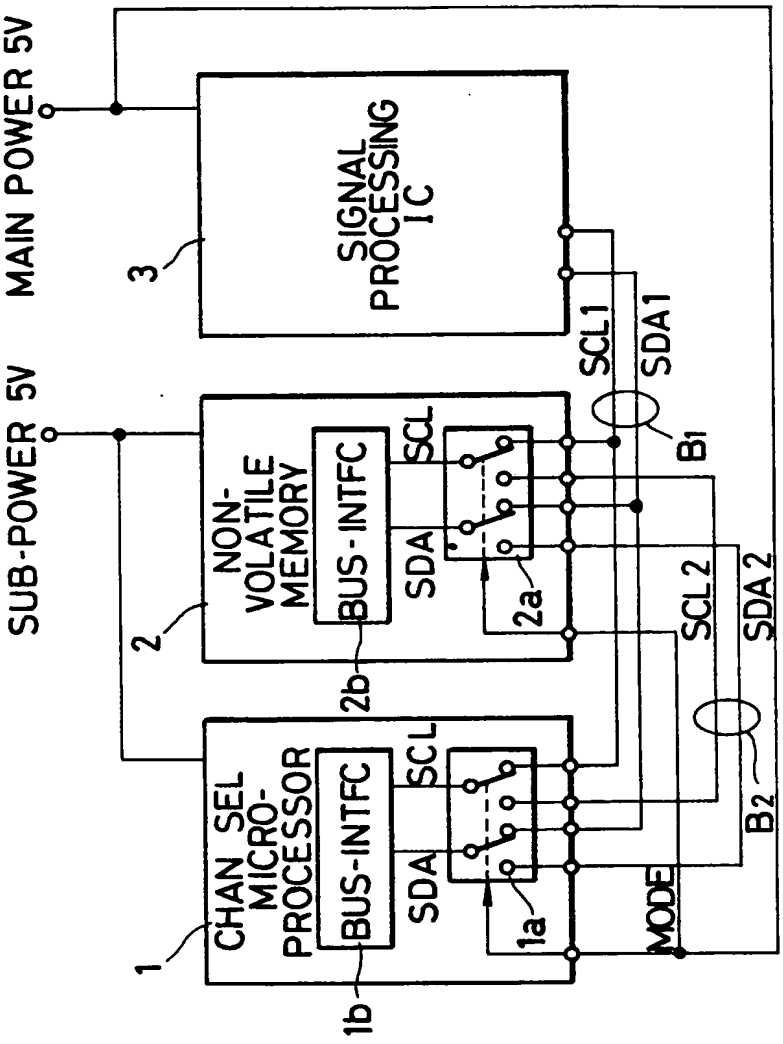

MAIN POWER 5V
SUB-POWER 5V
SIGNAL PROCESSING I C
3
NON-VOLATILE MEMORY
BUS-INTFC
SCL
SDA
2
2a
2b
CHAN SEL MICRO-PROCESSOR
BUS-INTFC
SCL
SDA
1
1a
1b
SCL1
SDA1
B1
SCL2
SDA2
B2
MODE

FIG.2

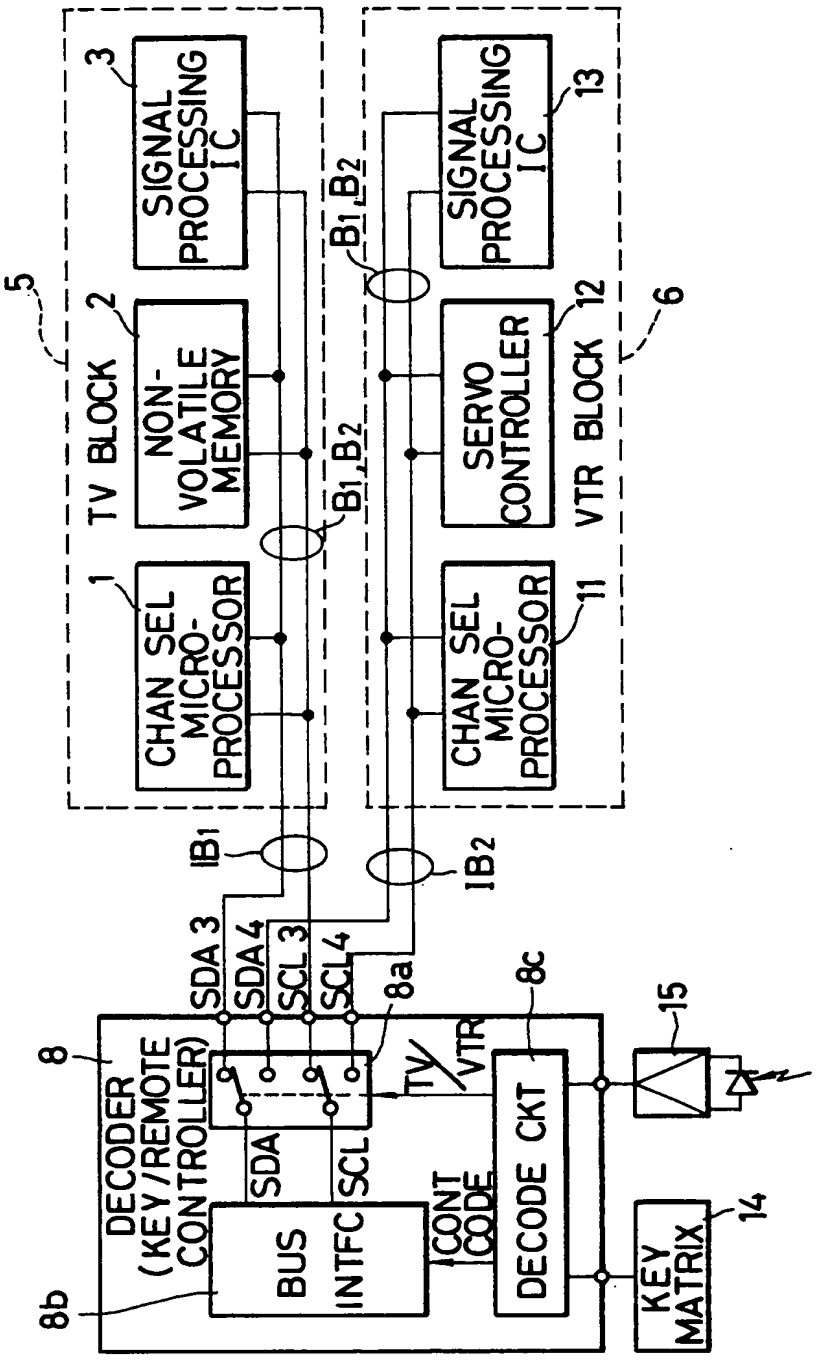

5
TV BLOCK
1
CHAN SEL MICRO-PROCESSOR
2
NON-VOLATILE MEMORY
3
SIGNAL PROCESSING I C
6
VTR BLOCK
11
CHAN SEL MICRO-PROCESSOR
12
SERVO CONTROLLER
13
SIGNAL PROCESSING I C
B1, B2
B1, B2
IB1
IB2
SDA 3
SDA 4
SCL 3
SCL 4
8a
8c
15
8
DECODER (KEY/REMOTE CONTROLLER)
TV
VTR
SDA
SCL
BUS INTFC
CONT CODE
DECODE CKT
KEY MATRIX
14
8b

FIG.3

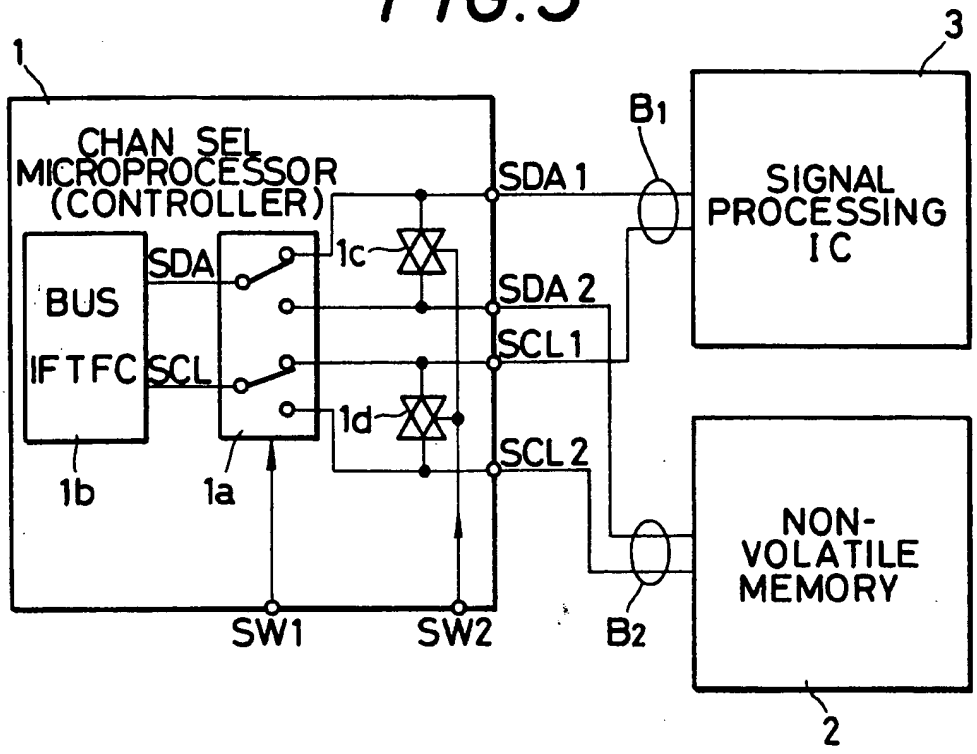
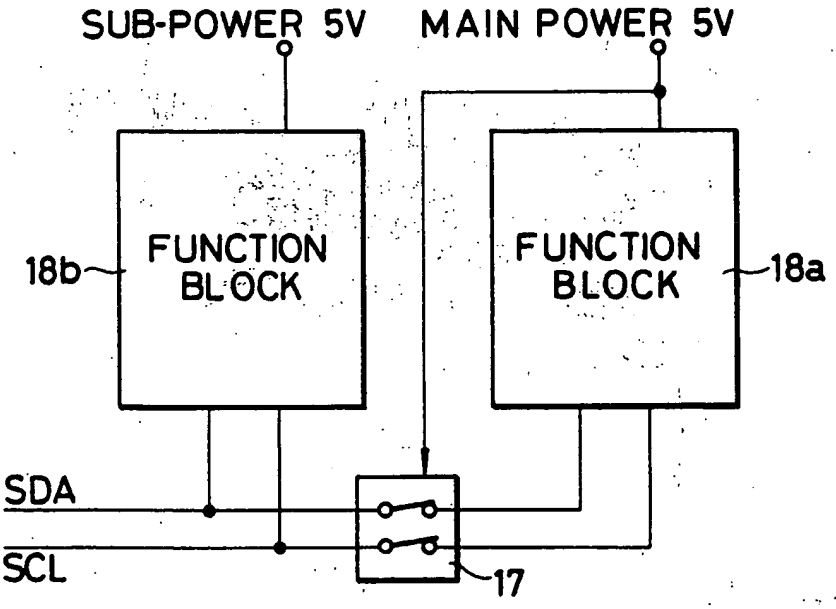

1
3
CHAN SEL
MICROPROCESSOR
(CONTROLLER)
BUS
IFTFC
SDA
SCL
1c
1d
1b
1a
SDA1
SDA2
SCL1
SCL2
B1
B2
SIGNAL
PROCESSING
IC
NON-
VOLATILE
MEMORY
SW1
SW2
2

FIG.4


SUB-POWER 5V
MAIN POWER 5V
18b
FUNCTION
BLOCK
FUNCTION
BLOCK
18a
SDA
SCL
17